REMARKS

Applicants acknowledge with appreciation the courtesy of the several telephone conversations with Examiner Parekh at which time the outstanding official action, which is a final rejection, was discussed as well as the scheduling of an interview. The Examiner indicated that his supervisor needed to be present at the interview and was unavailable. During a further telephone conversation with the Examiner, possible amendments to the claims to place the application in allowance were discussed and the Examiner recommended that a Request for Continuing Examination (RCE) be prepared along with an amendment and after which, the possibility of an interview would be considered. Accordingly, applicants submit herewith amended claims and a Request for Continuing Examination in this application.

Claims 17-30 have been canceled from the application without prejudice or disclaimer and new claims 31-44 have been added. These claims essentially parallel claims 17-30 and are fully supported by applicants' specification.

More particularly, claim 31 specifies the single semiconductor package as fully supported by applicants' specification and as may clearly be seen from Fig. 5H. As may be seen from this figure, the semiconductor package consists of an unsupported single layer linearly consisting of at least two solder mask portions (12) at selected locations and between and adjacent said solder mask portions is a die pad (14) which forms a portion of the layer. This die pad is adjacent to and contiguous to the solder mask portion of the layer. The lead layer (13) forms a portion of the linear layer and is adjacent to and contiguous with the solder mask portions of the layer. A chip adheres to the surface of the die pad portion by a silver paste. Electrical connectors (5) attach from the chip to the lead layers, all of which are covered with a molded resin. Fig. 5H shows the intermediate support layer which is shown in Fig. 5G, removed. Applicants most respectfully submit that all the claims now present in the application are now in full compliance with 35 U.S.C. § 112 and are clearly patentable over the references of

record. Rejection of claims 17 and 23 under 35 U.S.C. § 102(b) as being anticipated by Fukutomi et al. has been carefully considered but is most respectfully traversed.

In the official action, it is urged that Fukutomi et al. discloses a single semiconductor package comprising a solder mask/resist layer (8 in Fig. 10g) formed at selected locations, a lead/connection layer being an intermediate and contiguous thereto, the solder mask/resist layer and a die pad layer having a chip adhering to the die pad layer. Applicants have carefully considered this disclosure and clearly, there is no anticipation as is evident from a comparison of Fig. 5H of the present application as reflected in Applicants' claims and Fig. 10g of the patent as well as the disclosure of this figure at column 13 of the patent.

In this regard, it is to be noted that additional layers are presented not shown in the figure. See for example column 13 at line 13 where it is indicated that a nickel layer of 0.001 mm in thickness **(not shown in Fig. 10)** is present on one side of an electrolytic copper foil 1 of 0.35 mm in thickness. Note also line 38 of this column for the teaching that a photosensitive dry film was again laminated on the back side of the copper foil, and an etching pattern was formed by using the registration marks 18. Thereafter, the copper foil 1 and the nickel layer were etched to form the copper foil 1 into bumps 7 and to expose the wiring portion. These are clearly features not present in the presently claimed invention and therefore, there is no anticipation of claims 31 and 38 present in the application. Accordingly, it is most respectfully requested that this rejection be withdrawn.

The rejection of claims 18-22 and 24-30 under 35 U.S.C. § 103(a) as being unpatentable over Fukutomi et al. in view of Kawahara et al. has been carefully considered but is most respectfully traversed for the reasons discussed above.

It is urged in the official action that regarding claim 18, Fukutomi et al. discloses using the solder mask/resist, insulating material but fails to specify using the material being selected from the group consisting of polyimide and UV-curable resins. For the reasons discussed above and the amendments to the claims, clearly, the Fukutomi et al. reference does not disclose the required solder mask resist, insulating material of

the present invention. Therefore, the teaching of the insulating material does not overcome this rejection. The necessary motivation is absent from the prior art and Applicants' specification may not be relied upon to provide the necessary motivation to modify the references to arrive at the presently claimed invention. Therefore, this aspect of the rejection is most respectfully traversed.

The same reasoning applies to the rejection of claims 19 and 21 and this aspect of the rejection is most respectfully traversed in view of the amendments to the claims and the above comments.

With respect to claim 20, it is urged that Fukutomi et al. disclose forming the solder mask by coating and that applicants' claim 20 does not distinguish over Fukutomi regardless of the process of forming the solder mask, because only the final product is relevant, not the process of making such as coating or photo-processing. It is most respectfully submitted that the present invention discloses a semiconductor package without a substrate for reducing the package thickness and enhancing production yield. In order to achieve these objectives, the present invention provides an interim substrate covered by a solder mask at selected areas. The surfaces of the interim substrate that are not covered by the solder mask have a plurality of lead layers and die pad layers formed thereon at selected locations. The interim substrate provides a firm support base for bonding wires soldering on the lead wires during the wire bond processing. After the molding process is completed and singulation processes are finished, the interim substrate is removed by an etching process.

The reference discloses semiconductor packages which do have substrates. The claim limitations with respect to the process are not being relied upon and it is believed that the amendment claims clearly distinguish over the prior art despite any processing limitations. It is to be noted that the examiner has indicated that the process is patentably distinct from the product and restriction has been required in the parent application. Clearly, it is most respectfully requested that this rejection be withdrawn.

In view of the above comments and amendments to the claims, favorable reconsideration and allowance of the above-identified application is now in order and is most respectfully requested.

Respectfully submitted,
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